It is believed that a fee of $0 is due. ***The Assistant Commissioner is authorized to deduct said fees under 37 C.F.R. §§ 1.16 to 1.21 from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT3992.*** *Should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT3992. In the event the monies in that account are insufficient, the Assistant Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/*2000/050,800 .

IN THE DRAWINGS

It is noted that the drawings filed on July 11, 2000 are accepted by the Examiner.

IN THE CLAIMS

1. (Previously amended) A system, comprising:

a power supply configured to provide a standby signal and receive a power up signal;

a detection circuit coupled to receive the standby signal and output a power on signal for the power supply in response to receiving the standby signal;

a delay circuit coupled to receive the power on signal, wherein the delay circuit is configured to provide the power up signal to the power supply after a predetermined delay in response to receiving the power on signal; and

a stabilizer circuit coupled between the standby signal and the power up signal, wherein the stabilizer circuit is configured to provide a stable transition in the receipt of the power up signal; and

wherein the delay circuit is configured to provide the delayed power on signal to the power supply as the power up signal once the predetermined period of time has passed since the delay circuit received the power on signal; and

wherein the stabilizer circuit is further configured to receive the standby signal and to provide the standby signal to the power supply as the power up signal to keep the power up signal inactive.

2. (Cancelled)

3. (Previously amended) The system of claim 1, further comprising:

an integrated circuit coupled to receive the standby signal from the power supply.

4. (Previously amended) A system, comprising:

a detection circuit configured to receive a standby signal from a power supply and to deliver a control signal;

a delay circuit coupled to receive the control signal and to deliver a delayed control signal for the power supply in response to the control signal after a predetermined period of time;

a stabilizer circuit configured to receive the standby signal and to receive the delayed control signal, wherein the stabilizer circuit is further configured to provide the delayed control signal to the power supply to ensure a stable transition during the receipt of the delayed control signal by the power supply.

5. (Cancelled)

6. (Original) The system of claim 4, further comprising:

the power supply coupled to provide the standby signal to the detection circuit, wherein the power supply is further coupled to receive the delayed control signal.

7. (Original) A system, comprising:

a delay circuit configured to receive a standby signal from a power supply, wherein the delay circuit is configured to deliver a delayed standby signal a predetermined period of time after receiving the standby signal ; and

a detection circuit configured to receive the delayed standby signal, wherein the detection circuit is configured to deliver a control signal for a power supply in response to receiving the delayed standby signal.

8. (Original) The system of claim 7, further comprising;

a stabilizer circuit configured to receive the standby signal and to receive the control signal, wherein the stabilizer circuit is further configured to provide the control signal to the power supply to ensure a stable transition during the receipt of the control signal by the power supply.

9. (Original) The system of claim 7, further comprising:

the power supply coupled to provide the standby signal to the delay circuit, wherein the power supply is further coupled to receive the control signal.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Previously amended) A system, comprising:

an integrated circuit;

a power supply coupled to provide power to the integrated circuit, wherein the power supply is further configured to provide a standby signal to the integrated circuit, wherein the power supply is further configured to receive a power up signal;

a detection circuit coupled to receive the standby signal, wherein the detection circuit is configured to output a power on signal for the power supply in response to receiving the standby signal;

a delay circuit coupled to receive the power on signal for the power supply from the detection circuit, wherein the delay circuit is configured to output a delayed power on signal for the power supply in response to receiving the power on signal after a predetermined period of time; and

a stabilizer circuit coupled between the delay circuit and the power supply, wherein the stabilizer circuit is configured to receive the delayed power on signal and to provide the delayed power on signal to the power supply for the delay circuit, wherein the stabilizer circuit is further configured to provide a stable transition from inactive to active for the power up signal at a power supply; and

wherein the delay circuit is configured to provide the delayed power on signal to the power supply as the power up signal once the predetermined period of time has passed since the delay circuit received the power on signal; and

wherein the stabilizer circuit is further configured to receive the standby signal and to provide the standby signal to the power supply as the power up signal to keep the power up signal inactive.

18. (Cancelled)

19. (Cancelled)